

SYSTEMVERILOG

ADVANCED VERIFICATION FOR FPGA DESIGN

DESCRIPTION

Modern FPGA designs have tremendously advanced in both performance and capacity. Verification of this kind of designs has become a daunting task, especially the validation of the design against the specification and test plan.

SystemVerilog provides a comprehensive set of verification tools and is a natural extension to Verilog. It also provides constructs with clearer intent like enumerated types, integrated assertions and higher language constructs, which support design hierarchy and Object Oriented Programming (OOP). Powerful testbench features allow for more flexible and reusable testbench development, even in the context of a VHDL based design.

This workshop will give an overview about the SystemVerilog language and will introduce into new verification methodologies „Assertion Based Verification“, „Constrained Random Generation“ and „Functional Coverage“. The participant will learn how to use these powerful verification tools to speed up verification as well as to measure the verification progress and how these methodologies can be naturally applied to the verification of VHDL designs.

SHORT AGENDA

- ▶ Motivation
- ▶ Introduction to SystemVerilog
- ▶ SystemVerilog Assertions
- ▶ Constrained Randomization
- ▶ Functional Coverage

TARGET GROUP

FPGA design and verification engineers

PREREQUISITES

Experience with VHDL or Verilog for Design and Verification

DURATION

3 days

LANGUAGES

English or German

COURSE TARGETS

- ▶ Basic knowledge of SystemVerilog
- ▶ Basics of OOP in SystemVerilog
- ▶ Use of OOP for faster and more efficient, reusable testbench designs
- ▶ Knowledge of the concept of an automated testbench
- ▶ Introduction to assertions, constrained randomization and functional coverage

COSTS

upon request

www.trias-mikro.com



CONTACT

TRAINER

Alexandru Vlad Velea

has an Electronics, Telecommunications and Information Technology University degree followed by MBA postgraduate degree.

From 2005 on he has been covering mostly the following Siemens products:

- HDL design, simulation and synthesis
- Wiring and harness design

He has a bright knowledge as consultant/ advisor/ technical support/ tools trainer. He is Wiring Harness consultant/ advisor for the Mentor Graphics / Siemens tools since 2011 and Digital IC flow (design/ simulation/ synthesis) consultant/ advisor for the Mentor Graphics/ Siemens tools starting 2005.

TRIAS is an Expert Partner of Siemens Digital Industries Software. Siemens Digital Industries Software awards the status "Expert" to sales partners who have in-depth expert knowledge in a product area or industry and have proven this repeatedly in reference projects.

Alexandru Vlad Velea is certified by Siemens for the products Capital | Capital Essentials (formerly VeSys®) for the automotive and aerospace (Aero) markets and continuously undergoes a mandatory certification program to verify and expand his competencies.

ADDITIONAL COURSES

- ▶ UVM Made Easy for FPGA Designer
- ▶ VHDL 2008
- ▶ Verilog for VHDL User

Subject to change



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