TRIAS TRAINING CENTER

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Issue 05| 2024

TRIAS
a vargroup company

ABOUT US

As TRIAS mikroelektronik GmbH, we have been gathering experience since 1989 to offer innovative product solutions for design automation (EDA) in the areas of FPGA and IC design | verification, as well as for ECAD in the form of a model-based E/E system development platform for the development, production and service of wire harnesses and wiring systems.

As Cadlog and part of the Vargroup - the European market leader for the distribution of high-quality IT solutions - and the associated expansion of the product range such as PCB design and cybersecurity, we are working towards the common goal of digitalisation in electronics.

Our mission is to support you with our broad expertise and experience in your digitalisation in product development, from the product idea to the delivery of the product, so that you can exploit the full potential of these technologies.

WE SUPPORT YOU IN YOUR DIGITAL TRANSFORMATION.

Note

Click on the spot ● in the header on the following pages for more information.

TRIAS TRAINING CENTER

TRIAS TRAININGS

Training is an important topic and so we train our customers in innovative design and verification processes as well as in the use of our EDA and ECAD solutions. Our Training Center educates our customers on FPGA design and verification, high-level languages (HDL) and signal integrity and also offers tool training. Thus, we make an important contribution to digitalization in product development.

- SystemVerilog – "Advanced Verification" for FPGA Design
- VHDL 2008
- Verilog for VHDL Users
- UVM Testbench Made Easy
- Accelerating FPGA and Digital ASIC Design
- Accelerating FPGA VHDL Verification and introducing UVVM

- Signal Integrity in PCB Design
- Design and validation of DDR interfaces on PCBs

- Tool Trainings for tools by Siemens EDA – formerly Mentor Graphic and Siemens Digitial Industries Software

TRIAS TRAININGS

SYSTEMVERILOG – "ADVANCED VERIFICATION" FOR FPGA DESIGN

This workshop will provide an overview about the language SystemVerilog and introduce the new verification methodologies „Assertion Based Verification", „Constrained Random Generation" and „Functional Coverage". Participants will learn how to use these powerful tools to speed up verification as well as to measure the verification progress and how these methodologies can be naturally applied to the verification of VHDL designs.

VHDL 2008

The VHDL 2008 training course provides an overview about the changes and enhancements added to the language by the standard IEEE 1076-2008. The training is structured in three main areas, that cover new and changed synthesizable constructs, verification constructs that have been added coming from PSL (IEEE 1850). And in the final section the course will give an overview about how constrained randomization and functional coverage, which are not natively supported by the language, can be used with the OSVVM library.

VERILOG FOR VHDL USER

As designs become more complex and development times shrink, development teams increasingly need to leverage IP cores. This means that engineers must become "language-neutral" when dealing with HDL languages. They need a solid knowledge of VHDL and Verilog and the related design techniques.

Our workshop, with its fast and effective method, is suitable for experienced VHDL users to understand the differences, but also the similarities between VHDL and Verilog, and to master the Verilog-specific issues that could otherwise lead to difficult-to-identify problems.

We offer public, live online and on-site training.

For more information, visit our website at

Training

So, they are always up to date.

TRIAS SCHULUNGEN

UVM TESTBENCH MADE EASY

Due to the complexity of the UVM library, creating a testbench is a time consuming task and requires extensive knowledge of the capabilities offered by the library. To support verification engineers in the initial creation of a testbench infrastructure, the UVM framework was developed to create a UVM testbench very quickly. This can be simulated immediately and is adapted to the use case by making changes in some places using application-specific code.
After a short introduction to some UVM classes and expressions, the workshop UVM TESTBENCH EASY quickly turns to the details of the UVM framework.
The course is aimed at verification engineers with no prior UVM knowledge who want to get started using UVM testbenches.
The goal of the course is to create a complete UVM testbench using the Siemens EDA UVM Framework (UVMF), which is then supplemented with application-specific code in a few places.

ACCELERATING FPGA AND DIGITAL ASIC DESIGN

Implementing an FPGA or ASIC design does not just depend on knowing an HDL language. In addition to the knowledge of all language constructs, it is also important to structure the implementation in a suitable manner and to know advantages and disadvantages of different descriptions of the same behavior. If such approaches are consistently used, it will avoid many problems, which take a lot of time for causes to be found and solved, and thus reach their destination faster. The course will show how the development can be optimized and accelerated and also the quality of the design be improved.

- *Course in English language*

We also offer training as a live|online course - starting with one participant.

For more information, visit our website at

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TRIAS TRAINING

ACCELERATING FPGA VHDL VERIFICATION AND INTRODUCING UVVM

A significant part of the time for any FPGA project is taken up by verification. Reducing this time will accelerate the entire project development. The key to this is a well-structured testbench. This course focuses on FPGA verification and teaches how to build a testbench in a structured way. Theory alternates with practical examples and hands-on tutorials. It also covers important topics such as coverage, BFMs, debugging and randomization. This course contains a general introduction to modern verification methodology and to UVVM (Universal VHDL Verification Methodology) – the world-wide #1 VHDL-FPGA verification methodology, and also the fastest growing verification methodology independent of HDL.

- *Course in English language*
- *Knowledge of VHDL prerequisite*.

SIGNAL INTEGRITY IN PCB DESIGN

This workshop is aimed at developers, who want to develop high-speed interfaces between semiconductor components, and complex board-level high-speed circuits. The training is suitable for developers, who not only design schematics, but also systems and layout. They will learn to judge when signal integrity becomes important, and relevant, e.g. to select the appropriate termination procedure. Signal reflection, and crosstalk effects are described, and demonstrated by simulation. Simulation examples are also demonstrated for common memory interfaces. You will learn how to implement high-speed bus systems, including clock design, load, and signal termination. In addition, the power distribution, and short circuits in the design are important issues.

- *As an optional training module the topics signal integrity issues and solutions for high-speed memory interfaces, and serial transceiver links can be offered.*

All courses are constantly revised.

For more information, visit our website at

Training

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TRIAS TRAINING

DESIGN AND VALIDATION OF DDR INTERFACES ON PCBs

This workshop is for developers who want to implement high-speed memory interfaces on custom boards. Memory interfaces are very often used, they are faster and faster - and design problems are becoming more and more challenging. The training is suitable for developers who design not only schematics, but also systems and layout. You will become familiar with the peculiarities of memory modules for logical and physical designs.

Time and voltage tolerances are discussed. You will learn how to use signal integrity simulation to optimize the high-speed memory interfaces. IBIS models and simulation will reveal the effects and possible problem areas. You will learn how to implement high-speed memory slots, including on-board topics. In addition, the power supply problems are discussed. Finally, you will get to know board-level verification options.

All courses are constantly revised.

For more information, visit our website at

Training

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TRIAS TRAINING

TOOL TRAININGS FOR TOOLS BY SIEMENS EDA – FORMERLY MENTOR GRAPHICS AND SIEMENS DIGITAL INDUSTRIES SOFTWARE

We are pleased to offer a range of tool trainings that can also be tailored to your individual needs:

MODELSIM/QUESTA CORE: HDL SIMULATION

ModelSim /Questa Core: HDL Simulation teaches users new to using ModelSim or Questa SIM for HDL simulation how to effectively use ModelSim/Questa Core to verify VHDL, Verilog, SystemVerilog, and mixed HDL designs.

MODELSIM/QUESTA CORE: ADVANCED TOPICS

ModelSim/Questa Core: Advanced Topics teaches you to capitalize on the extensive capabilities of ModelSim/Questa Core to effectively and efficiently analyze and debug digital HDL designs.

CAPITAL HARNESS XC

The Capital Harness XC course introduces users to the basic and more complex functionality within the Capital Harness XC product. This tool provides a seamless transition of data from Capital Logic or Capital Integrator into Capital Harness XC.
Capital Harness XC demonstrates how to pull mechanical data from third party MCAD tools into Capital Harness XC. The course also demonstrates how to create and maintain individual design objects (e.g., wires, multicores, clips, connectors, etc.) within the harness diagrams.

This is only a small part of the list of available tool trainings, we are happy to inform and advise you on our entire offer.

All courses are constantly revised.

For more information, visit our website at

Training

So, they are always up to date.

TRIAS TRAINING

CAPITAL WIRING DESIGNER ESSENTIALS

This course introduces the Capital Essentials | former VeSys suite of applications, and helps you understand Capital Wiring Designer Essentials functionality. We're going to dive into the steps involved in creating, editing, and wiring a schematic design, using this tool. We'll also go through how to use Capital Wiring Designer Essentials to create multi level multicores, daisy chains, highways, stacked pins, and use footprints, as well as some Design Management.

CAPITAL HARNESS DESIGNER ESSENTIALS

This course supports designers and engineers working on harness design and manufacturing. Attendees will be introduced to the Capital Essentials | former VeSys environments and Capital Harness Designer Essentials functionality.

CAPITAL LOGIC AERO

Capital Logic Aero teaches you how to create projects, create and maintain design and diagram structure, create shared objects, set object naming preferences, set option definitions, create revisions and build lists, create functional diagrams, handle shared objects in and across diagrams, place conductors,assign options and library parts, compare designs, create library components, report on designs created.

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Training

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TRIAS TRAINING

CAPITAL LOGIC DESIGNER AERO

The Capital Logic Designer - Aero course introduces users to the basic and more complex functionality within the Capital Logic Designer product for aero customers. In this course, you will learn how to create projects, create and maintain design and diagram structure, create Shared objects, set object naming preferences, set option definitions, create revisions and build lists, create Functional Diagrams, handle shared objects in and across diagrams, place conductors, assign options and library parts, compare designs, create library components, and report on designs created.

CAPITAL LOGIC DESIGNER GENERATIVE

In this course you learn how Capital Logic Designer fits within your organization's generative design flow of the wiring design process. Designers and engineers will learn how to create projects, create and maintain design and diagram structure, create shared objects, set object naming preferences, set option definitions, create revisions and build lists, create functional diagrams, handle shared objects in and across diagrams, place conductors, assign options and library parts, compare designs, create library components, and report on designs created.

CAPITAL LOGIC DESIGNER INTERACTIVE

In the Capital Logic Designer Interactive course, designers and engineers will learn how to create their schematic and wiring designs with our 'correct by constructions' design methods. Students will learn how to create projects, create and maintain design and diagram structure, create Shared Objects, set object naming preferences, set option definitions, create revisions and Build Lists, create Wire Diagrams, how to handle Shared Objects in and across diagrams, place Conductors, assign Options and Library Parts, compare designs, and how to report on designs created.

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TRAINER

Alexandru Vlad Velea
has a Electronics, Telecommunications and Information Technology University degree followed by MBA postgraduate degree.

From 2005 on he has been covering mostly the following Siemens products:
• HDL design, simulation and synthesis
• Wiring and harness design

He has a bright knowledge as consultant/ advisor/ technical support/ tools trainer. He is Wiring Harness consultant/ advisor for the Mentor Graphics / Siemens tools since 2011 and Digital IC flow (design/ simulation/ synthesis) consultant/ advisor for the Mentor Graphics/ Siemens tools starting 2005.

TRIAS is an Expert Partner of Siemens Digital Industries Software. Siemens Digital Industries Software awards the status "Expert" to sales partners who have in-depth expert knowledge in a product area or industry and have proven this repeatedly in reference projects.

Alexandru Vlad Velea is certified by Siemens for the products Capital | Capital Essentials (formerly VeSys®) for the automotive and aerospace (Aero) markets and continuously undergoes a mandatory certification program to verify and expand his competencies.

COURSES

- SystemVerilog – Advanced Verification for FPGA Design
- VHDL 2008
- Verilog for VHDL Users
- UVM Made Easy for FPGA Designer
- Tool trainings for tools by Siemens EDA
- Trainings for Capital™ and Capital™ Essentials

TRAINER

Dr.-Ing. Jürgen Wolde

studied theoretical electrical engineering and graduated with a degree in engineering.
He then completed his doctorate in the field of electromagnetic compatibility to become a Doctor of Engineering. This followed the transition into the industry where he worked until 2005 in communications engineering at Alcatel. The scope ranged from ASIC design for products, to
assembly designs and complex research designs using FPGA-based boards. Collaboration on a variety of studies and research projects, and management activities rounded off the range of applications.

He has been self employed since 2006, and has become a long-time partner of PLC2, TRIAS and other companies, where he works as a technical trainer worldwide. Jürgen Wolde is also the co-author of numerous presentations and scientific publications as well as co-owner of several patents.

COURSES

- **Signal Integrity in PCB Design**
- **Design and validation of DDR Interfaces on PCBs**

TRAINER

Espen Tallaksen

is the CEO and founder of the newly established EmLogic and previously also Bitvis, both independent design centres for embedded software and FPGA, - with Bitvis as a leading Nordic company within its field and EmLogic soon to be. He graduated from the University of Glasgow (Scotland) in 1987 and has 30 years' experience with FPGA and ASIC development from Philips Semiconductors in Switzerland and various companies in Norway. During twenty years Espen has had a special interest for methodology cultivation and pragmatic efficiency and quality improvement.

One result of this interest is the UVVM verification platform that is the #1 VHDL verification methodology and library world-wide, and in fact the fastest growing FPGA verification methodology independent of HDL.

He is giving courses world-wide on how to design and verify FPGAs more efficiently and with a better quality.

COURSES

- Accelerating FPGA and Digital ASIC Design
- Accelerating FPGA VHDL Verification

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