

VHDL-2008

DESCRIPTION

The VHDL 2008 training course provides an overview about the changes and enhancements added to the language by the standard IEEE 1076-2008. The training is structured in three main areas, that cover new and changed synthesizable constructs, verification constructs that have been added coming from PSL (IEEE 1850). And in the final section the course will give an overview about how constrained randomization and functional coverage, which are not natively supported by the language, can be used with the OSVVM library.

The attendee will learn the new and improved constructs for RTL design. In addition the new Assertion-Based Verification (ABV) methodology, coming from the PSL (IEEE 1850) language, will be discussed in detail complemented with the constrained randomization and function coverage additions that OSVVM provides. In hands-on labs the attendee will have the opportunity to use the enhanced language constructs, create assertions that describe specific sequential signal pattern, which are to be monitored for occurrence and for correctness, and to write randomized stimulus, and data oriented coverage models that will track the data values sent to the DUT.

AGENDA

- ▶ New and enhanced Features
 - ▶ Enhanced Generics
 - ▶ Hierarchical referencing
 - ▶ etc.
- ▶ Functional Verification : ABV
 - ▶ Layers
 - ▶ Boolean Expressions;
 - ▶ Temporal Expressions
 - ▶ Directives
 - ▶ Vunits
- ▶ Open Source VHDL Verification Methodology (OSVVM)
 - ▶ Randomizing using RandomPkg
 - ▶ Functional Coverage Using CoveragePkg
 - ▶ etc.

TARGET GROUP

Engineers with VHDL knowledge or basic knowledge of digital hardware design

PREREQUISITES

Basic knowledge of digital hardware design and good knowledge of VHDL

DURATION

2 days

LANGUAGES

English or German

COURSE TARGETS

- ▶ Mastering the new design capabilities and applying them on design examples
- ▶ Understanding of new verification features and how to use them in the own environment

COSTS

€ 1.400,00 per participant*

www.trias-mikro.com

**Including training materials*



CONTACT

TRAINER

Alexandru Vlad Velea

has an Electronics, Telecommunications and Information Technology University degree followed by MBA postgraduate degree.

From 2005 on he has been covering mostly the following Siemens products:

- HDL design, simulation and synthesis
- Wiring and harness design

He has a bright knowledge as consultant/ advisor/ technical support/ tools trainer. He is Wiring Harness consultant/ advisor for the Mentor Graphics / Siemens tools since 2011 and Digital IC flow (design/ simulation/ synthesis) consultant/ advisor for the Mentor Graphics/ Siemens tools starting 2005.

TRIAS is an Expert Partner of Siemens Digital Industries Software. Siemens Digital Industries Software awards the status "Expert" to sales partners who have in-depth expert knowledge in a product area or industry and have proven this repeatedly in reference projects.

Alexandru Vlad Velea is certified by Siemens for the products Capital | Capital Essentials (formerly VeSys®) for the automotive and aerospace (Aero) markets and continuously undergoes a mandatory certification program to verify and expand his competencies.

ADDITIONAL COURSES

- ▶ **SystemVerilog – Advanced Verification for FPGA Design**
- ▶ **VHDL 2008**
- ▶ **UVM Testbench Made Easy for FPGA Designers**

Subject to change



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