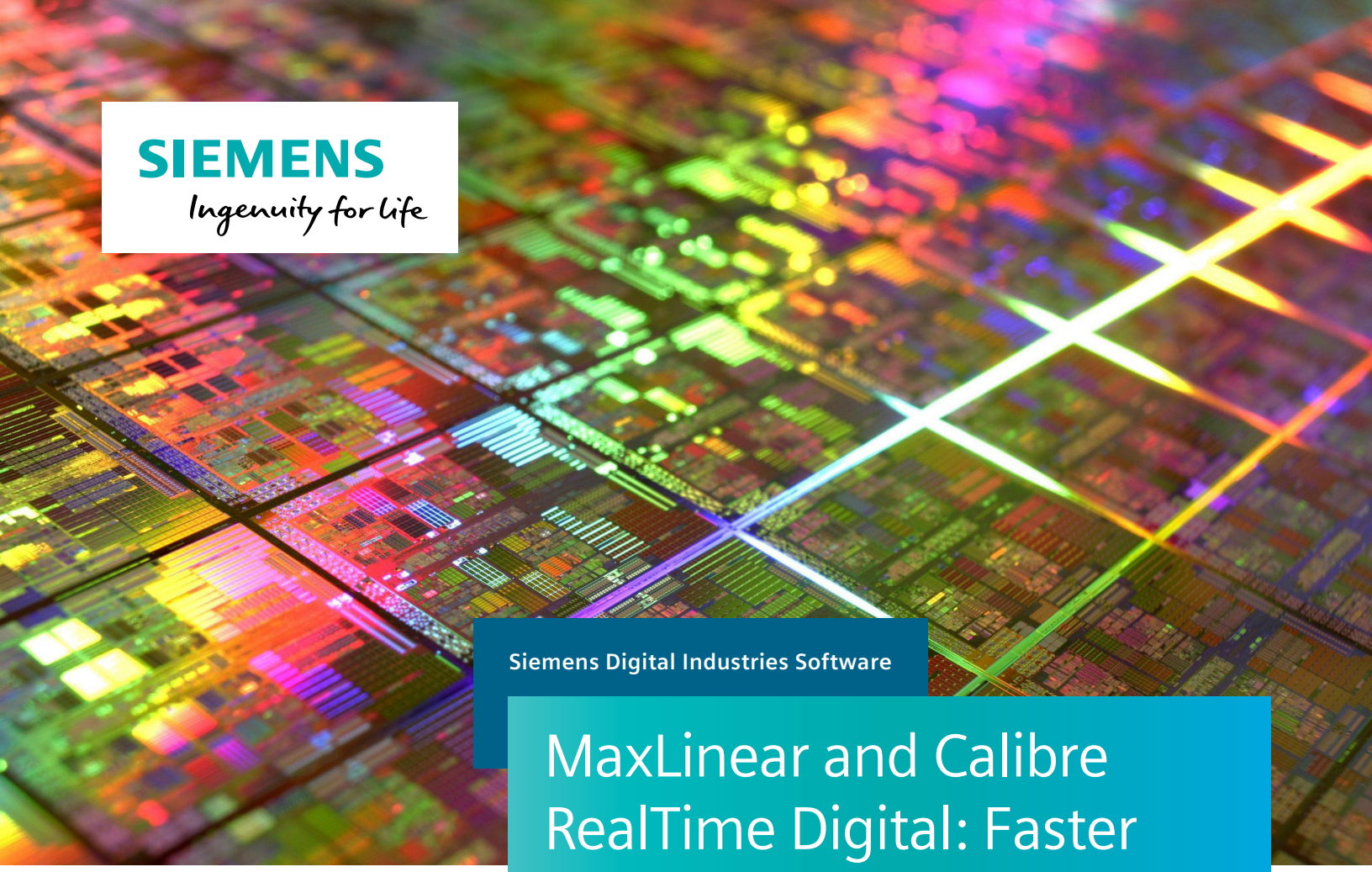

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MaxLinear and Calibre RealTime Digital: Faster signoff DRC convergence plus design optimization for manufacturability

Design to Silicon

MaxLinear implemented the Calibre RealTime Digital interface for fast, iterative, signoff DRC checking and fixing during floorplanning and placement. They not only reduce the total of batch DRC iterations, but also eliminate potential late-stage issues during final physical verification signoff that are exponentially harder to fix. Adopting the Calibre RealTime Digital interface enabled MaxLinear designers to accelerate their DRC closure and save weeks in their tapeout schedules for all designs at all nodes.

Srinivas Velivala
Siemens EDA

Introduction

MaxLinear, Inc. is a pioneer of low-power CMOS radio frequency (RF) and analog/mixed-signal (AMS) integrated circuits (ICs) for the connected home, wired and wireless infrastructures, and industrial and multi-market applications. One market focus is their digital signal processing (DSP) system-on-chip (SoC) solution, addressing the high-speed optical interconnect needs of mega-scale cloud and enterprise data centers. DSP chips for the server market are expected to work for 10 years or more, meaning both reliability and manufacturability are critical components of a successful design process.

Place and route (P&R) engineers at MaxLinear strive to achieve high reliability and manufacturability in their SoC designs, while also optimizing their power, performance, and area (PPA) design goals. However, automated design enhancements during P&R can create layout variances that lead to complex design rule checking (DRC) errors at the chip level, such as top-level/intellectual property (IP) blocks interface, or "last mile" functional/timing engineering change order (ECO) errors. The intricacy of these types of errors typically require P&R engineers to manually debug and correct during DRC closure.

Traditionally, batch DRC flows are set up for full-chip runs, and are not optimized for immediate DRC feedback on select design windows. In their effort to minimize debugging time while still ensuring correct-by-construction accuracy, P&R engineers at MaxLinear saw an opportunity to optimize their digital implementation physical verification process by using Calibre® RealTime Digital in-design DRC to enable on-demand Calibre signoff DRC within the P&R environment.

MaxLinear's design challenges and opportunities

MaxLinear's chips contain both analog and digital components. Because analog designs do not require many layers for the routing connections, MaxLinear optimizes the number of layers available for routing to reduce the overall cost of manufacturing. However, by increasing routing density in all layers uniformly, this layer optimization can make routing the digital designs challenging, and typically requires additional signoff DRC iterations to achieve DRC closure.

While native P&R DRC engines are designed to fix a majority of the DRC errors, the violations they don't address are typically complex DRC errors that require many manual debugging and DRC iterations to fix, a process that can take weeks and potentially delay tapeout schedules. After fixes are made using a local window, designers must manually merge the P&R data with IP data to generate a merged GDSII/OASIS database, and then run full batch DRC to verify this fixes. If DRC errors still exist, this time-consuming process must be repeated again and again.

These challenges are compounded by the inability of the P&R DRC solutions to recognize and flag some types of DRC violations, such as those introduced by:

- Manual DRC error fixes
- Last-minute functional/timing ECO changes
- Final via swaps made to improve DFM scores

MaxLinear wanted a flow that improves their DRC closure time, and enables their designers to meet both design reliability and manufacturability requirements, as well as PPA design goals. The Calibre RealTime Digital interface provides direct calls to Calibre analysis engines running foundry-qualified signoff Calibre rule decks (figure 1). These engines perform fast, incremental checking near shapes being edited, providing nearly instantaneous feedback on DRC violations. This immediate feedback in the P&R domain enables MaxLinear engineers to implement and check fixes with signoff quality, but without the need for full DRC iterations. With the ability to perform rapid, signoff-quality in-design fixing, they can achieve shorter DRC closure cycle times while still ensuring Calibre signoff DRC confidence.

We'll look at three areas where MaxLinear was able to use the Calibre RealTime Digital in-design DRC to improve design quality while reducing design closure time.

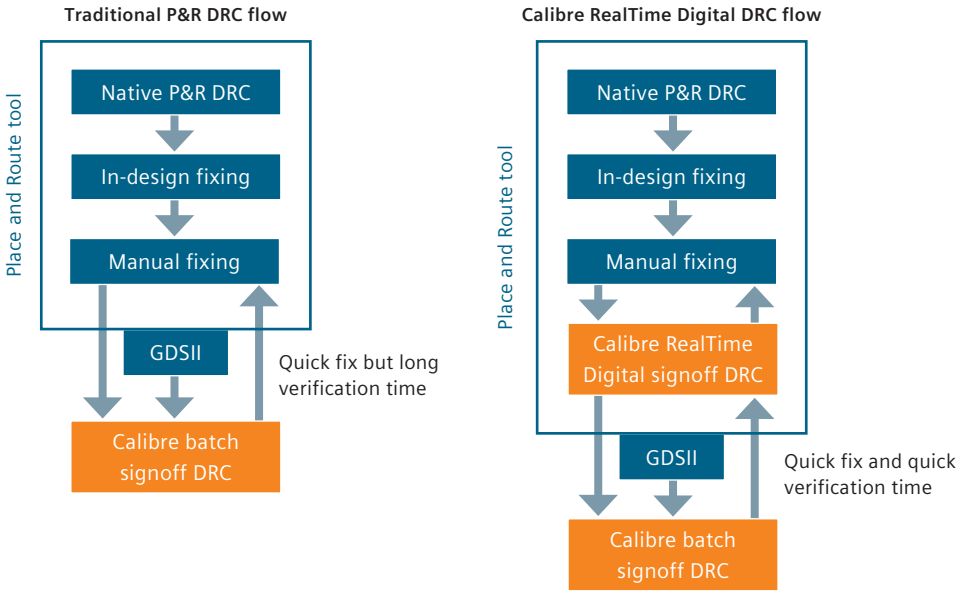


Figure 1: Traditional P&R DRC flow compared to the Calibre RealTime Digital in-design signoff DRC flow.

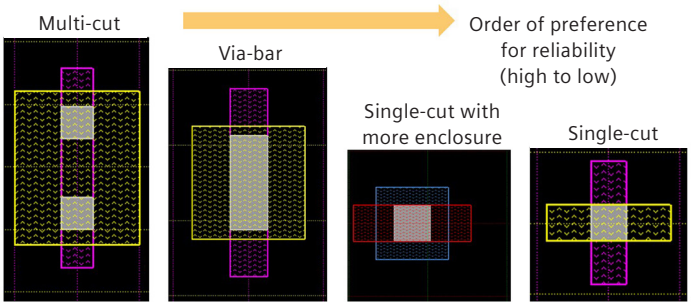
Via selection

P&R engineers at MaxLinear strive to achieve at least an 80% design for manufacturing (DFM) via score, a challenging task that requires selecting the best type of via in a given design area to address timing, reliability, and manufacturability.

Foundries typically provide four types of vias: single-cut, single-cut with extended enclosure, via-bar, and multi-cut (figure 2). Of these via types, the single cut is the least desirable because it has high resistance, negatively affecting timing, and its design for manufacturing (DFM) ranking is low. However, it does make routing easier, which leads

to fewer DRC errors. Single-cut vias with more enclosure added around the vias provide a better DFM ranking than the single-cut via, but they still have high resistance. Via-bars provide a high DFM ranking and better timing (because of the decrease in resistance), but make routing more challenging. Multi-cut vias provide the best reliability because they have two via shapes (making it unlikely that the vias will fail during manufacturing), and they provide improved performance benefits vs. both single-cut vias. However, they have the same routability challenges as the via-bar.

MaxLinear's preferred solution during digital design implementation is to maximize the use of multi-cut and via-bar vias to ensure that their designs meet timing, reliability, and manufacturability requirements. However, both multi-cut and via-bar types make routing the design more challenging, creating complex DRC errors that must be fixed manually, extending DRC closure time. With Calibre RealTime Digital in-design DRC, engineers can swap in new via types, use the in-design DRC in a local window to catch any DRC errors created by the swap, apply fixes, and then quickly validate again to ensure the layout is DRC-clean. They can also recheck DFM scores after completing multiple via swaps, typically when they are confident they are near or have achieved their target DFM score.



Via types	Routing	DFM ranking	Timing (Resistance)	Preferred order for reliability
Multi-cut	More routing tracks	High	High	1
Via-bar	More routing tracks	High	High	2
Single-cut with More closure	Medium routing tracks	Medium	Low	3
Single-cut	Fewer routing tracks	Low	Low	4

Figure 2: Preferred selection of via types for improving DFM ranking and timing.

Multi-patterning violations

Swapping out a single cut via for a multi-cut or via-bar via can also cause multi-patterning (MP) violations (figure 3) that can be challenging and time-consuming to fix, as they typically involve performing a what-if analysis on the layout by making a manual fix and then waiting for DRC feedback. The Calibre RealTime Digital interface enables P&R engineers to perform these what-if analyses quickly and confidently by providing immediate signoff DRC feedback on each manual edit, helping P&R engineers determine and implement the optimum fix for the MP violation.

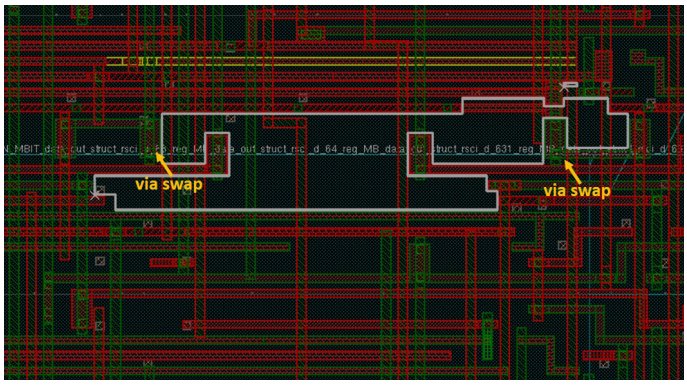


Figure 3: Single to multi-cut via swap causes an MP violation that can be manually fixed and immediately validated using Calibre RealTime Digital in-design DRC, improving designer productivity and saving overall DRC closure time.

Last-mile DRC closure

Moving to a new advanced technology node generally causes the area of the standard cells to shrink by ~55%. However, the area of the wires only shrinks by ~30%, leading to an increase in pin density. This increased density makes it difficult for the P&R routing engine to access the pins during routing without causing DRC errors. This challenge becomes even steeper for MaxLinear, because they intentionally use a limited set of routing layers to reduce manufacturing costs, which uniformly increases routing density across all layers.

Spacing violations

Figure 4 shows diagonal via spacing violations created during routing to AOI and OAI cells. To fix these types of spacing violations, designers must move the vias while ensuring no new DRC violation is generated.

By using the Calibre RealTime Digital interface to get immediate feedback on manual DRC fixes (figure 5), MaxLinear P&R engineers were able to quickly implement an optimum fix with confidence that they were not creating another DRC violation.

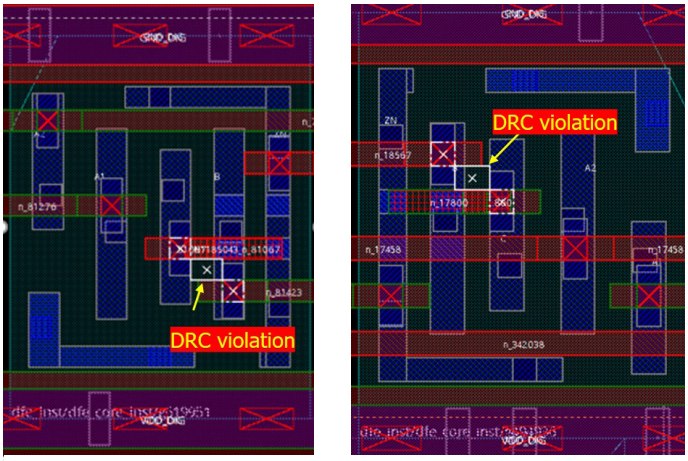


Figure 4: AOI and OAI cells with high pin density lead to DRC violations.

```
P&R >> Timing: DRC data preparation: 573 ms
Calibre RealTime is running DRC using configuration: "Default configuration"
DRC analysis window:      {8288123 24913022} {8289761 24914452}
DRC COMPLETE. TOTAL CHECK COUNT = 2457 TOTAL RESULT COUNT = 1 TOTAL ORIGINAL GEOMETRY COUNT = 649
Timing: Total run time: 1,627 ms
Timing: Total run time for 1 configuration: 3,968 ms
```

Figure 5: The Calibre RealTime Digital in-design DRC provides immediate signoff-quality feedback on placement violations for fast validation in the P&R environment.

ECO errors

Functional/timing signal shorts

Sometimes, when a design is close to tapeout, either a functional or timing error requires an ECO adjustment to the layout, which can result in a signal short (Figure 6). P&R engineers have two options for fixing this short: they can implement another ECO, or fix the short manually. Applying another ECO change can potentially affect the timing metrics of surrounding nets, as the router looks at the surrounding areas before making the required connectivity changes. P&R engineers typically prefer to manually fix the short to avoid any alteration to the surrounding nets. With the Calibre RealTime Digital interface, P&R engineers can manually fix the short in the P&R environment, and use the immediate DRC feedback to verify the fix.

Interface errors

In certain cases, an ECO change causes top-level and analog IP interface DRC errors. For example, tie-hi and tie-low signals are required in an IC, because not all inputs are used. To avoid glitches, unused inputs should be locked to a stable logic state, and not left floating. In the layout shown in figure 7, a functional ECO (netlist change) was required when the P&R engineers realized they had to connect the signal route to a pin in the analog IP that was originally a tie-low signal. This ECO change caused a DRC issue with the other port of the analog IP. MaxLinear P&R engineers determined the optimum way to fix this DRC error was with a manual correction, using the Calibre RealTime Digital interface to get immediate DRC feedback during the process to confirm the validity of the fix, and to ensure no new DRC errors were generated.

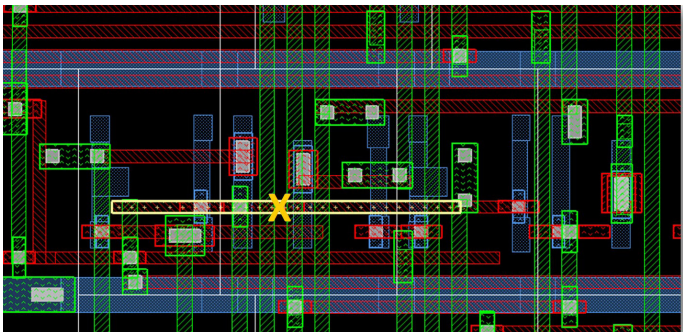


Figure 6: The signal short caused by an ECO adjustment can be manually fixed and then quickly verified in the P&R environment.

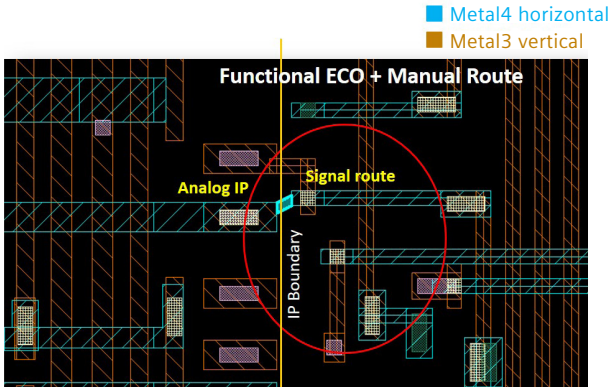


Figure 7: A functional ECO change resulted in a tie-low signal in IP being connected to top-level signal, creating IP/block interface DRC violations.

Signal EM issues

Close to tapeout, MaxLinear P&R engineers observed that the high-fanout and frequently switching nets (such as the clock net) were drawing excess current, which can lead to signal electromigration (EM) issues. On inspection, the engineers determined that the clock net was drawing high current because the router had inserted single-cut vias to avoid routability issues.

This EM violation only existed in part of the clock net path, not the entire net. Because a strong driver is driving high-fanout nets, the EM violation only happens on the driver side, not on the receiver side, as indicated by the arrows in Figure 8. Fixing this violation requires careful inspection of the design to determine whether to swap the single-cut vias with multi-cut vias or via-bars, or to convert the single width wire to double width to drive more current (figure 8). Once the design decision is made, the Calibre RealTime Digital interface provides immediate signoff DRC feedback to validate the manual edits, helping the engineers reach DRC closure quickly and efficiently.

Re-tapeout checks

Sometimes, after you have submitted your design to the foundry for manufacturing, unexpected ECO changes are required. When this occurs, the foundry mandates that you run special re-tapeout (RTO) checks before delivering the design with the ECO changes back to the foundry. These special checks must be run because the mask for the layer is already prepared, which adds more constraints to the location of your geometries. Tapeouts are typically done layer by layer. When ECO changes are made to metal layers, the foundry requires the design team to run the RTO checks on related layers as well. For example, if the ECO changes were on the Metal2 and Metal3 layers, designers would also need to run RTO checks on Via1 and Via3 layers.

The additional constraints imposed during RTO checks makes fixing DRC errors complex, and typically requires many DRC iterations, which significantly extend the time it takes to re-tapeout a design. MaxLinear P&R engineers used Calibre RealTime Digital checks to interactively verify their fixes for the RTO DRC issues, and were able to quickly deliver the design back to the foundry, resulting in direct cost savings.

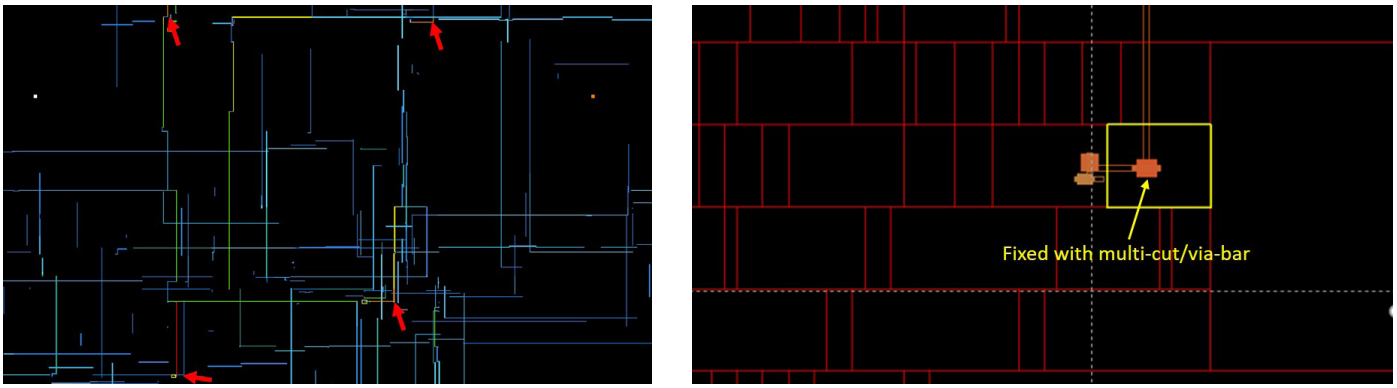


Figure 8: (Left) EM issues created on the high-toggle clock net because of a strong driver drawing high current are fixed (right) by swapping single vias with multi-cut or via-bar vias.

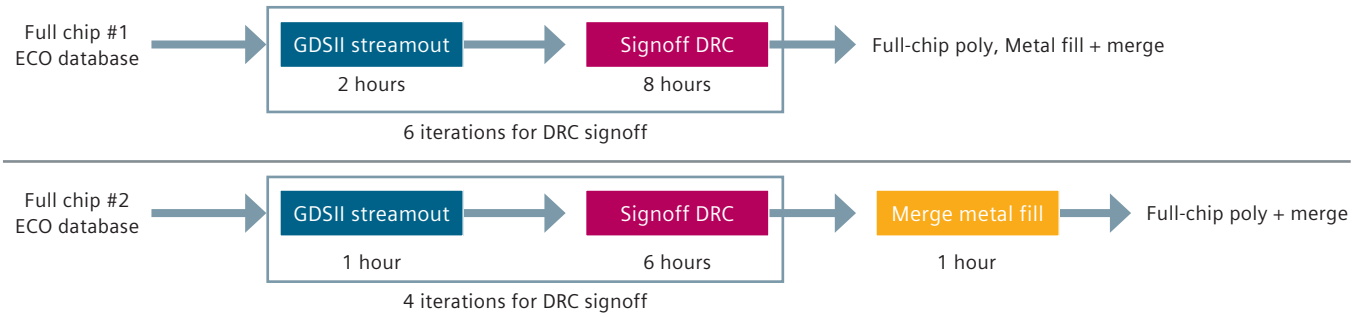
In Figure 9, an ECO change resulted in the vertical metal path moving to the left, creating via enclosure errors on a neighboring net, as the two signals are now closer to one other. The via enclosure errors are seen only when running the RTO checks. MaxLinear P&R engineers used the Calibre RealTime Digital in-design DRC to perform a quick what-if analysis on this design window and determine the optimum fix.

Figure 9: RTO via enclosure error due to ECO change after initial tapeout of specific design layers.

Results

The Calibre RealTime Digital interface enabled P&R engineers at MaxLinear to perform targeted, on-demand Calibre signoff DRC during the digital design flows, enabling them to meet their unique timing, reliability and manufacturability constraints, and save 50% over the previous physical verification closure time required for every design iteration across established and advanced process nodes (figure 10). The Calibre RealTime Digital interface easily plugs in and integrates with all major P&R tools, allowing P&R engineers to receive Calibre signoff-quality DRC feedback without leaving their P&R environment.

In addition to the runtime benefits, having immediate Calibre signoff DRC feedback means digital designers can quickly explore the effect of new or revised design rules in new technology nodes. No more tedious design rule interpretations—designers can simply run a rule and see the impact, enabling design companies to implement new designs and get them to market more quickly.



Sl. No	Block name	Technology	DRC count	Tapeout DRC run iteration	DRC closure w/o Calibre RTD (hours)	DRC closeure with Calibre RTD (hours)	Signoff time saved	Instances counts
1	Full chip 1	28nm	25	6	65 (60 + 5 for fix)	25 (20 + 5 for fix)	61%	25M
2	Full chip 2	16nm	12	4	65 (60 + 5 for fix)	25 (20 + 5 for fix)	42%	15M
3	Block	28nm	33	6	65 (60 + 5 for fix)	25 (20 + 5 for fix)	40%	5.2M

Figure 10: Runtime statistics demonstrate the benefits gained by using Calibre RealTime Digital in-design DRC at MaxLinear.

Conclusion

By enabling fast, iterative signoff DRC checking and fixing during floorplanning and placement, the Calibre RealTime Digital interface not only reduces batch DRC iterations, but also eliminates potential late-stage issues during final physical verification signoff that are exponentially harder to fix. The immediate DRC feedback provided by the Calibre RealTime Digital interface supports a correct-by-construction approach, while enabling digital designers to better focus on meeting their power, performance, and area (PPA) goals. Because the full range of Calibre physical verification capabilities is available, they can interactively explore the cause of a DRC error and perform what-if analysis to determine the optimum fix. Eliminating the need for multiple database stream-outs and batch DRC runs provides significant productivity advantages for "last mile" manual DRC closure, enabling digital designers to shave weeks off their tapeout schedule. In short, the Calibre RealTime Digital interface lets the designers drive DRC closure, not their tools.

Adopting the Calibre RealTime Digital interface enabled MaxLinear designers to accelerate their DRC closure and save weeks in their tapeout schedules for all designs at all nodes. For companies designing complex DSP SoC solutions, the ability to satisfy the high-speed optical interconnect needs of mega-scale cloud and enterprise data centers while maintaining high product reliability and product life, these advantages can make the difference between just being in the market, and being a market leader.

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