02|2021

TRIAS TRAINING CENTER

DESIGN AND VALIDATION OF DDR INTERFACES ON PCBs

DESCRIPTION

This workshop is aimed at developers, who want to implement high-speed memory interfaces on custom boards. Memory interfaces are used very often, they will be faster and faster – and the design issues are more and more challenging. This Workshop is designed for developers, who not only design schematics but also design systems and the layout.

Participants will learn the memory device specifics relevant for logical and physical design. Timing and voltage margins will be discussed.

The use of signal integrity simulation to optimize high-speed memory interfaces will be shown. IBIS models and simulation are used to explain the effects and potential bottlenecks. Participants will learn how to implement high-speed memory interfaces, including board level design topics. Furthermore power supply issues will covered and board level verification options.

AGENDA

- Introduction
- Overview Memory Devices
- DDRx Memory Devices Details
- Memory Controllers
- Memory Interface Design
- Short Introduction to Signal Integrity (SI)
- Basics for SI Simulation of Memory Interfaces
- SI Simulation Options for Memory Interfaces
- Improving Design Margins Through Simulation
- Verification of Memory Interfaces
- Memory Interface Guidelines
- Course Summary

TARGET GROUP

Hardware Design and CAD Engineers, who design HS Memory Interfaces I System Designers

PREREQUISITES

Basic knowledge of hardware design

DURATION

2 days

LANGUAGES

German or Englisch

COURSE TARGETS

- Understand memory timing relationships
- Learn basics of signal integrity and IBIS simulation
- Learn how to design memory interfaces
- Run signal integrity simulations to verify memory interfaces in design process
- Discuss options for hardware verification on existing hardware

COSTS

€ 1.250,00 per participant*

www.trias-micro.com

Including training materials, lunch and refreshments

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TRAINER

Dr.-Ing. Jürgen Wolde

studied theoretical electrical engineering graduated with a degree in engineering. He then completed his doctorate in the field of electromagnetic compatibility to become a Doctor of Engineering. This followed the transition into the industry, where he worked until 2005 in communications engineering at Alcatel. The scope ranged from ASIC design for products, to assembly designs and complex research designs using FPGA-based boards. Collaboration on a variety of studies and research projects and management activities rounded off the range of applications.

He has been self employed since 2006 and has become a long-time partner of the PLC2, TRIAS and other companies, where he works as a technical trainer worldwide. Jürgen Wolde is also the co-author of numerous presentations and scientific publications as well as co-owner of several patents.

ADDITIONAL COURSES

- Signal Integrity in PCB Design

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