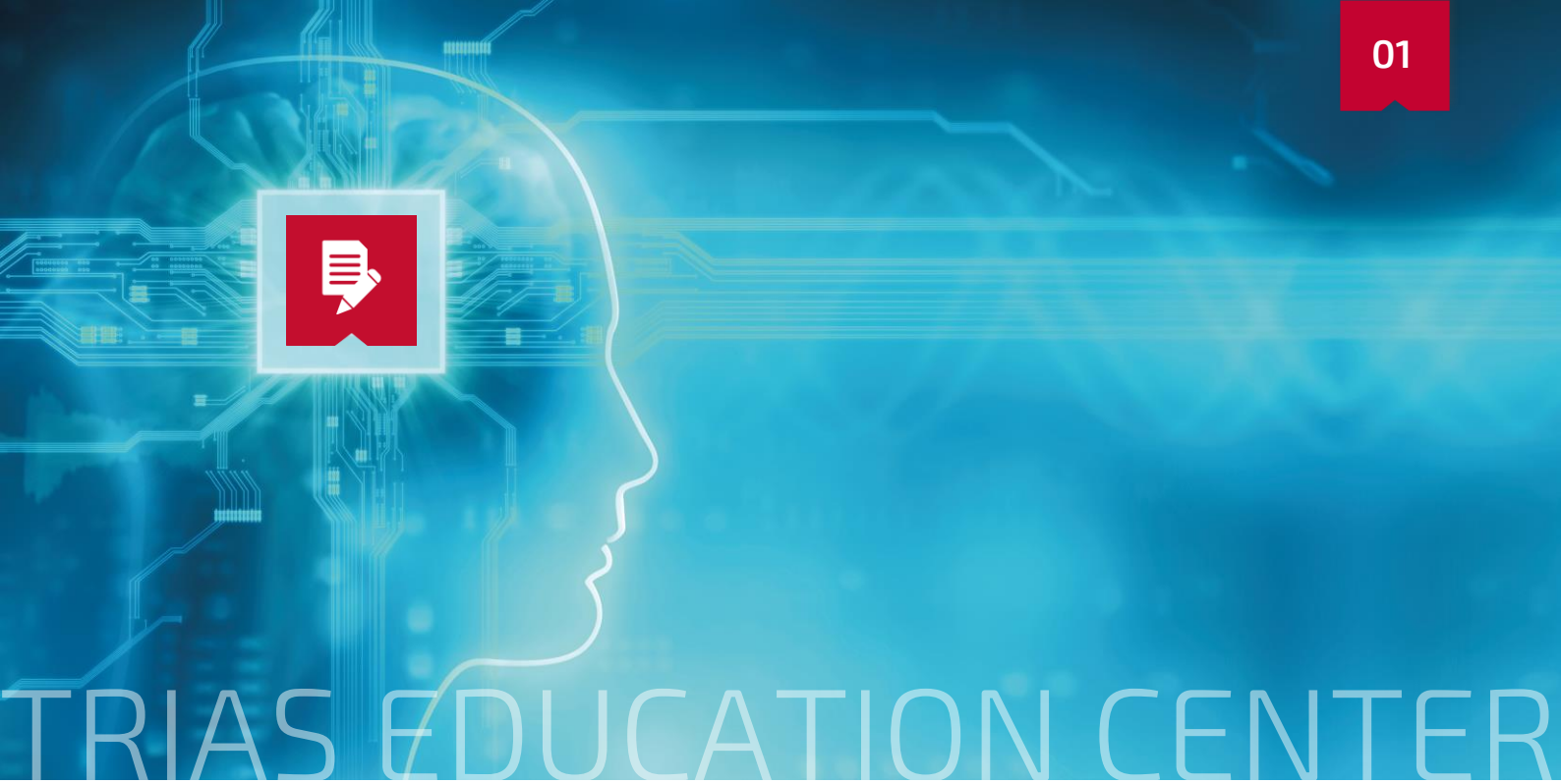
TRIAS EDUCATION CENTER

Issue: 02 | 2021

TRIAS mikroelektronik GmbH



TRIAS EDUCATION CENTER

TRIAS TRAINING

Founded in 1989, TRIAS mikroelektronik GmbH has become a leading distribution company in the fields of EDA (Electronic Design Automation), Lifecycle Management (ALM/PLM) solutions and ASIC solutions.

Our Education Center provides training for our customers in innovative design and verification processes, as well as in our EDA- and PLM solutions

- SystemVerilog – “Advanced Verification” for FPGA Design
- VHDL 2008
- Verilog for VHDL Users
- UVM Made Easy for FPGA Designer

- Signal Integrity in PCB Design
- Design and validation of DDR interfaces on PCBs

- Accelerating FPGA and Digital ASIC Design
- Accelerating FPGA VHDL Verification

- Product Training for tools by Mentor® A Siemens Business

TRIAS mikroelektronik GmbH | Moerser Landstraße 408 | Krefeld | Germany
Telefon: +49 [0] 2151.953.01-0 | Telefax: +49 [0] 2151.953.01-15 | E-Mail: info@trias-mikro.com | **www.trias-mikro.com**

TRIAS mikroelektronik GmbH

TRIAS TRAINING

SYSTEMVERILOG – "ADVANCED VERIFICATION" FOR FPGA DESIGN

This workshop will provide an overview about the language SystemVerilog and introduce the new verification methodologies „Assertion Based Verification", „Constrained Random Generation" and „Functional Coverage". Participants will learn how to use these powerful tools to speed up verification as well as to measure the verification progress and how these methodologies can be naturally applied to the verification of VHDL designs.

VHDL 2008

The VHDL 2008 training course provides an overview about the changes and enhancements added to the language by the standard IEEE 1076-2008. The training is structured in three main areas, that cover new and changed synthesizable constructs, verification constructs that have been added coming from PSL (IEEE 1850). And in the final section the course will give an overview about how constrained randomization and functional coverage, which are not natively supported by the language, can be used with the OSVVM library.

VERILOG FOR VHDL USER

As designs become more complex and development times shrink, development teams increasingly need to leverage IP cores. This means that engineers must become "language-neutral" when dealing with HDL languages. They need a solid knowledge of VHDL and Verilog and the related design techniques.

Our workshop, with its fast and effective method, is suitable for experienced VHDL users to understand the differences, but also the similarities between VHDL and Verilog, and to master the Verilog-specific issues that could otherwise lead to difficult-to-identify problems.

We offer public, live online and on-site training.

For more information, visit our website at

Training

TRIAS mikroelektronik GmbH | Moerser Landstraße 408 | Krefeld | Germany
Telefon: +49 [0] 2151.953.01-0 | Telefax: +49 [0] 2151.953.01-15 | E-Mail: info@trias-mikro.com | **www.trias-mikro.com**

TRIAS mikroelektronik GmbH

TRIAS TRAINING

SIGNAL INTEGRITY IN PCB DESIGN

This workshop is aimed at developers, who want to develop high-speed interfaces between semiconductor components, and complex board-level high-speed circuits. The training is suitable for developers, who not only design schematics, but also systems and layout. They will learn to judge when signal integrity becomes important, and relevant, e.g. to select the appropriate termination procedure. Signal reflection, and crosstalk effects are described, and demonstrated by simulation. Simulation examples are also demonstrated for common memory interfaces. You will learn how to implement high-speed bus systems, including clock design, load, and signal termination. In addition, the power distribution, and short circuits in the design are important issues.

- *As an optional training module the topics signal integrity issues and solutions for high-speed memory interfaces, and serial transceiver links can be offered.*

DESIGN AND VALIDATION OF DDR INTERFACES ON PCBs

This workshop is for developers who want to implement high-speed memory interfaces on custom boards. Memory interfaces are very often used, they are faster and faster - and design problems are becoming more and more challenging. The training is suitable for developers who design not only schematics, but also systems and layout. You will become familiar with the peculiarities of memory modules for logical and physical designs.

Time and voltage tolerances are discussed. You will learn how to use signal integrity simulation to optimize the high-speed memory interfaces. IBIS models and simulation will reveal the effects and possible problem areas. You will learn how to implement high-speed memory slots, including on-board topics. In addition, the power supply problems are discussed. Finally, you will get to know board-level verification options.

All courses are constantly revised.

We ensure they are always up to date.

For more information, visit our website at

Training

TRIAS mikroelektronik GmbH | Moerser Landstraße 408 | Krefeld | Germany
Telefon: +49 [0] 2151.953.01-0 | Telefax: +49 [0] 2151.953.01-15 | E-Mail: info@trias-mikro.com | **www.trias-mikro.com**

TRIAS mikroelektronik GmbH

TRIAS TRAINING

UVM MADE EASY FOR FPGA DESIGNER

Today's FPGA designs have become complex SoC type of designs, which has driven the complexity to a level that used to be specific to ASICs some years in the past. For a complete verification of those systems writing testbenches has become a challenging task. Different verification methodologies have addressed this on different levels. The most comprehensive approach is the Universal Verification Methodology, UVM. It has become a standard (IEEE 1800.2-2017). It provides SystemVerilog Verification base components that can be used to create a testbench infrastructure with a high reuse potential.

Since the UVM library is very complex building a testbench from scratch is a time-consuming task, and requires a good knowledge of the tools and the library provides. In order to help verification engineers to build a testbench infrastructure very quickly, UVM Framework has been developed. With UVM Framework a UVM testbench can be created very rapidly, and with a few changes the testbench is ready for simulation within a few hours.

The workshop UVM MADE EASY FOR FPGA DESIGNER will introduce to the most important UVM building blocks to provide a basic understanding how a UVM testbench looks like, how the component instance creation process works, and how the verification components communicate with each other and the DUT.

The attendees will create a UVM testbench with the UVM Framework in multiple steps for a simple example DUT during a hands-on lab that explains, and guides through the process until finally the testcase can be run. After this Workshop the attendee will be able to use the UVM Framework API to create a testbench infrastructure for his own FPGA design.

Course Targets

- *Verification - approaches and methodologies*
- *UVM - Fundamentals and Principles*
- *UVM Framework - Library Components, Structure, and API*

We offer training also as live online course - starting with 1 participant.

For more information, visit our website at

Training

TRIAS mikroelektronik GmbH | Moerser Landstraße 408 | Krefeld | Germany
Telefon: +49 [0] 2151.953.01-0 | Telefax: +49 [0] 2151.953.01-15 | E-Mail: info@trias-mikro.com | **www.trias-mikro.com**

TRIAS mikroelektronik GmbH

TRIAS TRAINING

ACCELERATING FPGA AND DIGITAL ASIC DESIGN

Digital design for FPGAs and ASICs has a huge improvement potential with respect to development time, and product quality.
A lot of time is wasted on inefficient design and lack of awareness and knowledge of the most critical digital design issues. This also seriously affects the quality of the end product. The really good thing is that this huge improvement potential can be realised just by making a few important changes to the way we design.
There will be a few examples on quite common bad approaches, and more examples on good approaches for architecture, CDC, Coding, Reuse, etc. Almost all examples are independent from both technology (FPGA/ASIC) and language (VHDL/Verilog/SystemVerilog).
The course is intended for FPGA designers and Digital ASIC designers, who wants to work smarter and more efficiently - and design products with higher quality.

.

The subjects of this English language course are:

- *Design Architecture & Structure*
- *Clock Domain Crossing*
- *Coding and General Digital Design*
- *Reuse and Design for Reuse*
- *Timing Closure*
- *Quality Assurance - at the right level*

ACCELERATING FPGA VHDL VERIFICATION

A significant part of the time for any FPGA project is taken up by verification. Reducing this time will accelerate the entire project development. The key to this is a well-structured testbench. This course focuses on FPGA verification and teaches how to build a testbench in a structured way. Theory alternates with practical examples and hands-on tutorials. It also covers important topics such as coverage, BFMs, debugging and randomization. This is also a great opportunity to get acquainted with the "Universal VHDL Verification Methodology" (UVVM), which is freely accessible as open source, allowing a well structured testbench to be easily and quickly created.

- *English language course*
- *Knowledge of VHDL prerequisite*.

All courses are constantly revised.

We ensure they are always up to date.

For more information, visit our website at

Training

TRIAS mikroelektronik GmbH | Moerser Landstraße 408 | Krefeld | Germany
Telefon: +49 [0] 2151.953.01-0 | Telefax: +49 [0] 2151.953.01-15 | E-Mail: info@trias-mikro.com | **www.trias-mikro.com**

TRIAS mikroelektronik GmbH

TRAINER

Hans-Jürgen Schwender

has a masters degree in electrical engineering. From 1991 until the end of 2001, he worked as an ASIC design engineer at Philips Kommunikationsindustrie and Lucent Technologies in Nuremberg and at Infineon Technologies in San Jose, CA, USA. He worked on the creation of specifications, the implementation in VHDL, verification on module and chip level as well as programming of ASIC Driver Software in C.

Mr. Schwender has been working at TRIAS mikroelektronik GmbH since 2002 and, as the technical manager covers a large part of Mentor's products - with a focus on HDL design, verification and cable harness design products.
.

TRIAS mikroelektronik GmbH

Moerser Landstraße 408
D-47802 Krefeld

+49 [0] 2151.95 301-0

+49 [0] 2151.95 301-15

info@trias-mikro.com

www.trias-mikro.com

COURSES

- SystemVerilog – Advanced Verification for FPGA Design
- VHDL 2008
- Verilog for VHDL Users
- UVM Made Easy for FPGA Designer

TRAINER

Dr.-Ing. Jürgen Wolde

studied theoretical electrical engineering and graduated with a degree in engineering. He then completed his doctorate in the field of electromagnetic compatibility to become a Doctor of Engineering. This followed the transition into the industry where he worked until 2005 in communications engineering at Alcatel. The scope ranged from ASIC design for products, to assembly designs and complex research designs using FPGA-based boards. Collaboration on a variety of studies and research projects, and management activities rounded off the range of applications.

He has been self employed since 2006, and has become a long-time partner of PLC2, TRIAS and other companies, where he works as a technical trainer worldwide. Jürgen Wolde is also the co-author of numerous presentations and scientific publications as well as co-owner of several patents.

TRIAS mikroelektronik GmbH

Moerser Landstraße 408
D-47802 Krefeld

+49 [0] 2151.95 301-0

+49 [0] 2151.95 301-15

info@trias-mikro.com

www.trias-mikro.com

COURSES

- Signal Integrity in PCB Design
- Design and validation of DDR Interfaces on PCBs

TRAINER

Espen Tallaksen

is the CEO and founder of the newly established EmLogic and previously also Bitvis, both independent design centres for embedded software and FPGA, - with Bitvis as a leading Nordic company within its field and EmLogic soon to be. He graduated from the University of Glasgow (Scotland) in 1987 and has 30 years' experience with FPGA and ASIC development from Philips Semiconductors in Switzerland and various companies in Norway. During twenty years Espen has had a special interest for methodology cultivation and pragmatic efficiency and quality improvement.

One result of this interest is the UVVM verification platform that is the #1 VHDL verification methodology and library world-wide, and in fact the fastest growing FPGA verification methodology independent of HDL.

He is giving courses world-wide on how to design and verify FPGAs more efficiently and with a better quality.

TRIAS mikroelektronik GmbH

Moerser Landstraße 408
D-47802 Krefeld

+49 [0] 2151.95 301-0

+49 [0] 2151.95 301-15

info@trias-mikro.com

www.trias-mikro.com

COURSES

- Accelerating FPGA and Digital ASIC Design
- Accelerating FPGA VHDL Verification

CONTACT

TRIAS
mikroelektronik GmbH

Moerser Landstraße 408
D-47802 Krefeld

+49 [0] 2151.95 301-0

+49 [0] 2151.95 301-15

info@trias-mikro.com

www.trias-mikro.com

In addition to the courses described we also offer product training for a number of tools by

Mentor®
A Siemens Business

Training