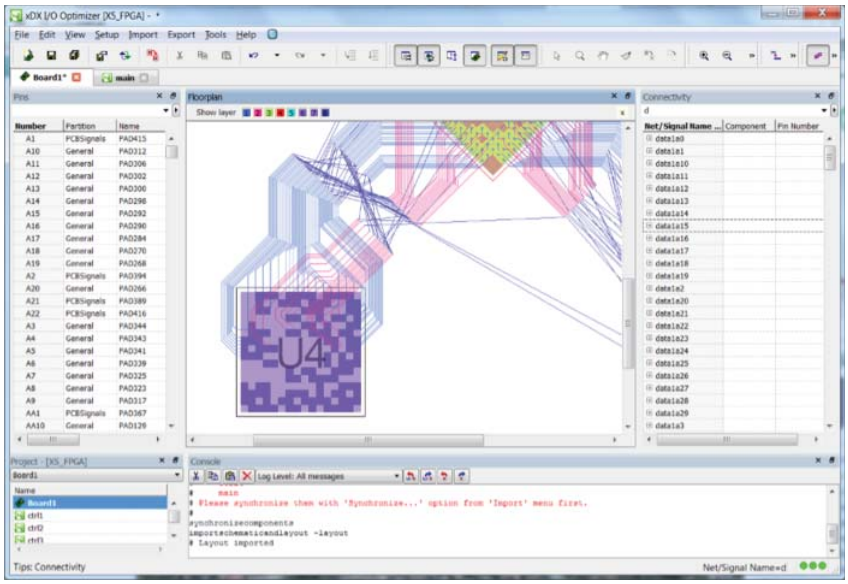
pads
personal automated design solutions

FPGA-PCB Co-Design Option

For PADS Professional



FPGA I/O optimizes pin-out assignments for improved routability and signal integrity.

MAJOR BENEFITS:

- Reduces total design time by using concurrent processes
- Decreases PCB manufacturing costs by eliminating PCB signal layers
- Eliminates PCB re-spins caused by out-of-date FPGA symbols on the PCB
- Utilizes high-speed performance optimization
- Removes costs associated with creating and maintaining FPGA symbol(s) for the PCB schematic

OVERVIEW

Today's powerful and extremely high pin-count FPGAs provide engineers with significant opportunities for increased features and functionality, while reducing the cost of their products. With this increased complexity comes significant challenges in integrating these devices onto the printed circuit board. Hundreds of logical signals need to be mapped to the physical pinout of the device while still maintaining the electrical integrity of the design. The increased complexity of the FPGAs also requires advanced synthesis technologies to reach timing closure faster, minimize the impact of design changes, and address application-specific requirements.

These challenges can be met with the optional FPGA-PCB optimization technology that adds HDL synthesis and advanced FPGA-PCB I/O optimization to PADS Professional. This interface between the HDL design environment and the physical implementation on the PCB significantly reduces both time-to-market and manufacturing costs.

The intuitive logic synthesis environment includes advanced optimization techniques, award-winning timing analysis, and advanced inferencing technology for vendor-independent design that accelerates time-to-market, eliminates design defects, and delivers superior quality of results (QoR).

FPGA I/O Optimization

Flow Integration

I/O optimization is tightly integrated with the PADS Professional design flow and is accessible at any stage of your project. Schematic, PCB Layout and FPGA databases are always synchronized which provides user control of the project's design data flow. In addition, schematic users can decide when the FPGA data (new or updated) is to be transferred to the PCB design.

Before PCB placement or routing is started, I/O optimization uses PADS project data for floor planning and better initial assignment. Results are exported to layout and FPGA parts are managed at either the project or enterprise library level.

Signal & Pin Assignments

Manually assigning hundreds of HDL signals to FPGA pins while still strictly adhering to the FPGA vendors' rules can be challenging. To simplify this process, PADS Professional delivers easy to use functionality for auto assignment, supervision of signal standards, assignment by simple drag & drop, support for operations on sets of objects, and dynamic filtering. Together, they make signal-pin assignment a simple operation. Every pin-assignment change is managed across the FPGA-PCB flow keeping it consistent, regardless of where the change is made.

Automated Part and Symbol Generation

The very nature of FPGA devices requires a different approach to the symbol generation process. FPGA logic typically changes many times during the project lifecycle and symbols must be kept consistent with those changes. With this advanced PADS option, you have a set of powerful features that makes symbol creation easy, fast, and error free, while still allowing full control of the symbol creation process. Compared to manual symbol creation, time is reduced from hours or days to minutes.

Floor Planning

An important phase of the PCB design flow is the component placement and orientation on the board layout itself. Floor planning can be done before and during the PCB layout process. This gives engineers and designers the clear advantage of being able to make FPGA pin assignment changes from the project's earliest stages, allowing optimized component placement and orientation, shortened net lines, and fewer net line cross-overs.

FPGA Multi Instance and Optimization

In most cases, the same FPGA device will have different logical functions across projects or even within a single project. PADS Professional I/O optimization automatically supports these situations during project development. FPGAs represented by different functional symbols in the BOM report are listed along with the vendor part numbers. Successful optimization of connections between two or more FPGA devices is almost impossible to perform manually. With this advanced PADS Professional option, an optimization algorithm evaluates all possible connection combinations to arrive at the optimum interconnect. Net crossovers arising from the initial assignment are also minimized, enabling higher route-completion rates.

FPGA Synthesis

Advanced Optimization Algorithms

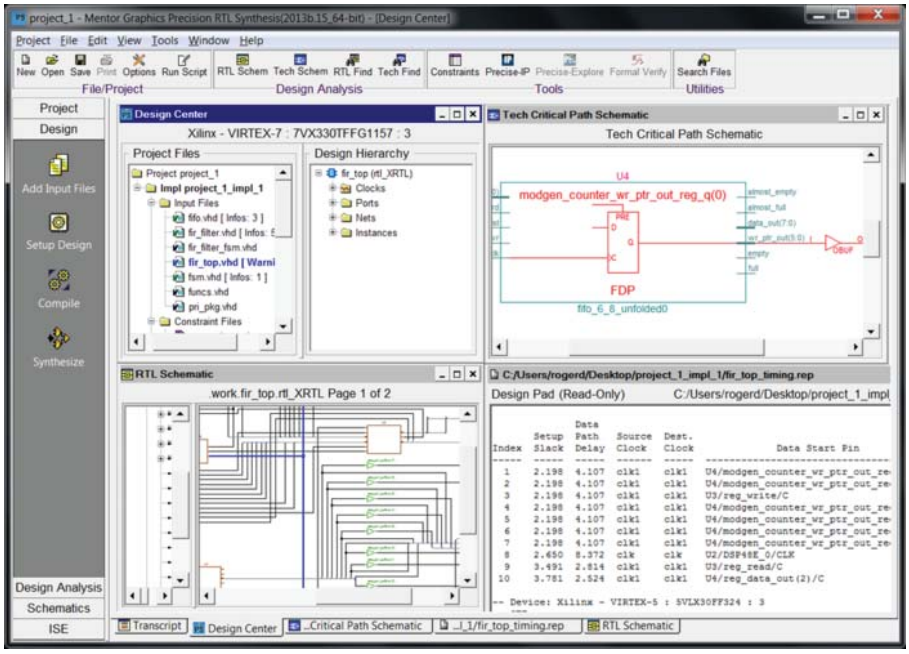
A suite of unique optimization algorithms automatically focuses specific optimizations on design areas that are most likely to hinder overall performance, such as finite state machines (FSM), cross-hierarchical paths, and paths with excessive combinational logic. These algorithms provide an automated, heuristic-based approach to delivering smaller and faster designs without the need for iterative manual intervention.

RTL & Technology Schematic Viewers

When the design is compiled, it is created with generic gates and viewed as an RTL schematic. After synthesis, a technology-mapped database is created with the technology schematic reflecting that database. Schematic viewers help you understand how the RTL is interpreted and mapped to the target FPGA technology.

Vendor Independence

Vendor-independent synthesis supports devices from Altera, Lattice, Microsemi, and Xilinx. Therefore, you may use the same HDL design source files and constraints to target any device and to obtain a synthesized netlist that can be used for place-and-route with the appropriate vendor tools. This vendor independence allows users to easily retarget and analyze results for any FPGA device, enabling you to find the best FPGA device for your design.



Advanced synthesis technologies, in a vendor-neutral environment, enable specific architectural optimization for each FPGA device.

All Device Support

In addition to supporting FPGA devices from the four leading FPGA vendors, the PADS FPGA-PCB co-design option also fully supports FPGA vendor tools such as Altera Quartus II, Lattice Diamond and ispLEVER, Microsemi Libero and Designer, and Xilinx ISE and Vivado.

Simple Constraints Flow

To accommodate today's highly complex FPGA design flows, a wide variety of constraint sources are supported, including those specified in HDL code, SDC files, and global constraints set within the tool itself. It is important to specify common timing constraints such as clock frequency, input/output delays, and timing exceptions (e.g.: multi-cycle and false paths during synthesis) to ensure optimal results from synthesis.

Gated Clock Conversions

ASIC designers typically use gated clocks for power management and other reasons. However, when mapped to FPGAs, these gated clocks can result in large clock skews, create glitches, and pose a timing analysis challenge. Gated clocks are converted automatically using the appropriate enable signals available in FPGAs.

DSP & RAM Inference Optimization

Today's advanced FPGA devices contain DSP and RAM embedded blocks in addition to normal logic blocks. This makes it critical for synthesis tools to understand a variety of RTL coding styles and map them to the appropriate DSP or RAM blocks for the best utilization of resources and performance. The PADS Professional FPGA-PCB Co-Design option has advanced inference and optimization capabilities to maximize the use of embedded resources for better area and frequency.

Verilog, SystemVerilog, & VHDL Support

With industry-leading language support for Verilog, SystemVerilog, and VHDL/VHDL-2008, designers may use any combination of these formats to create and synthesize RTL designs for optimal results.

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