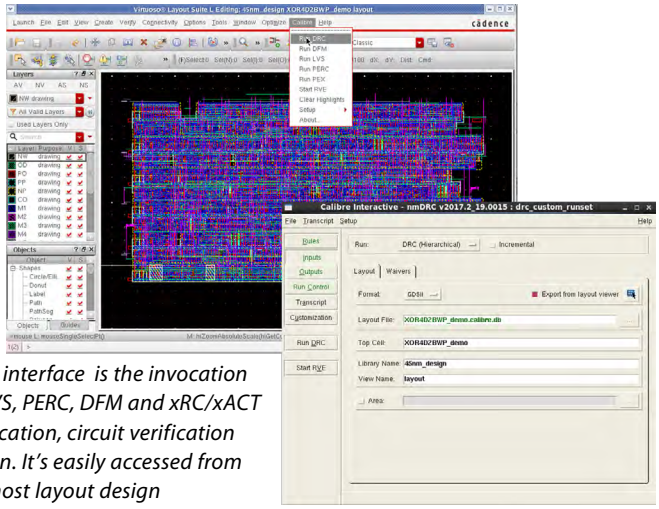
Push-Button Access to the Calibre Platform

Calibre Interactive

Physical Verification

D A T A S H E E T



The Calibre Interactive interface is the invocation GUI for Calibre DRC, LVS, PERC, DFM and xRC/xACT tools for physical verification, circuit verification and parasitic extraction. It's easily accessed from the menu bar within most layout design environments. The Calibre Interactive GUI also gives users access to the Calibre RVE interface , the robust and easy-to-use results viewing environment.

Calibre Interactive delivers push-button access to Calibre physical, circuit verification and parasitic extraction tools

The Calibre® Interactive™ interface provides users with fast and easy access to the Calibre tool suite, enabling designers to perform Calibre checking from within their familiar integrated circuit design environment. Designers using Mentor® Calibre DESIGNrev™ and Pyxis™, Cadence Design Systems® (Cadence) Virtuoso®, Encounter® and Innovus™, or Synopsys® IC Compiler™ (ICC), IC Compiler II (ICC2) or Laker™3 tools can adopt a single verification and extraction solution for their entire physical design flow, regardless of design style or methodology. Calibre offers a robust design-to-silicon tool suite for designers working with cell/block, full chip, analog, digital, analog/mixed signal, or systems-on-chip designs.

Single Verification Flow Solution

Because the Calibre Platform is independent of design styles, designers can use the Calibre Interactive interface to access and control all Calibre tools as a single physical/circuit verification and parasitic extraction flow for designs containing analog, digital, mixed signal or radio frequency (RF) components. The Calibre Interactive interface functions like your personal CAD engineer, providing infrastructure and a GUI to interactively set-up and manage configurations, rather than writing custom code. A single tool for physical and circuit verification in cell/block and full-chip eliminates the discrepancies caused by out-of-sync verification rules. It also eliminates maintenance associated with supporting multiple verification flows.

FEATURES AND BENEFITS:

Universal integration with layout and schematic evironments:

- Minimizes training and support overhead.
- Provides a single, consistent interface to lauch Calibre jobs across all your design tools.

Personal CAD engineer:

- GUI provides infrastructure to set up and manage configurations without writing custom code.

Runset options:

- Capture set-up for Calibre jobs in a single file, simplifying set-up maintenance and reproducibility.

Customized GUI options:

- Flexibility to customize the GUI for greater control over settings used in Calibre physical and circuit verification jobs.

Check Recipes:

- Create, configure and run individual subsets (recipes) of DRC and ERC checks.
- Share these recipes across multiple users.

Integrated Within Supported Layout Environments

Designers using Mentor Calibre DESIGNrev and Pyxis, Cadence Virtuoso, Encounter and Innovus, or Synopsys ICC, ICC2 and Laker3 tools can invoke the Calibre Interactive GUI to perform verification or extraction from within the design environment using the same rule file for cell/block or full chip.

Triggers

Triggers are a very powerful tool for customized integration. CAD teams can use pre- and post-execution triggers to run proprietary scripts before or after Calibre runs.

Customized GUI Options

CAD teams can define a customization file to generate a tailored Calibre Interactive GUI that gives users control over the Calibre execution. This file opens the customized GUI prior to opening the standard Calibre Interactive GUI. This GUI contains radio buttons and cyclical fields that users can select to control Calibre runs. CAD teams use customized GUIs to specify statements in the Calibre rules file, such as Define Select Check and variable statements.

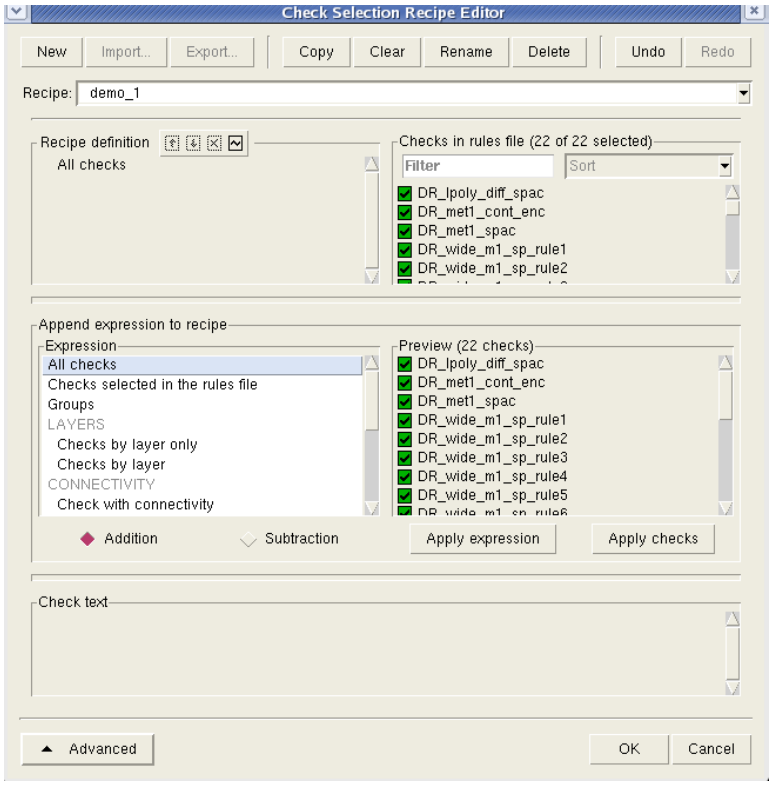
Runset Options

Calibre verification setup and runtime options can be captured as a template in a runset file to simplify the configuration, maintenance, and reproducibility of the setup (such as access to correct rule files, run directories, and other required settings). Using runsets eliminates common issues encountered when launching physical/circuit verification or parasitic extraction jobs.

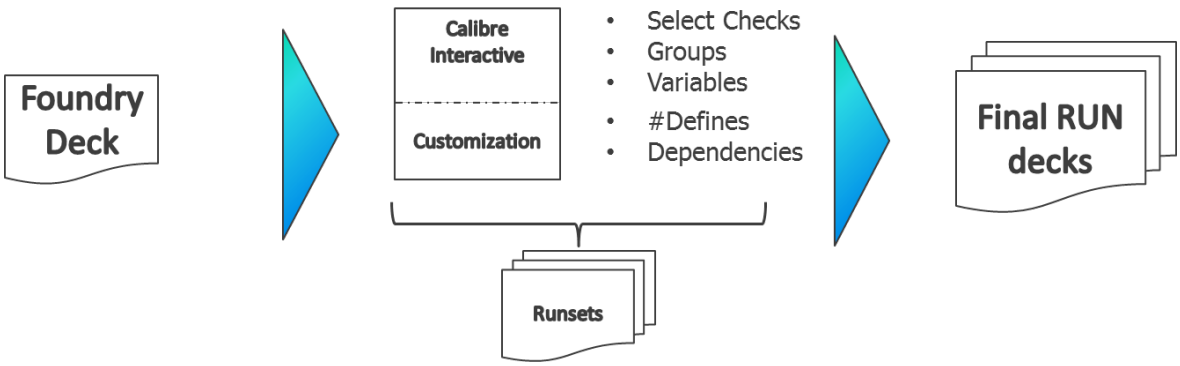
Design Rule Checking and Check Recipes

Designers can specify and run individual design rule checks (DRC) or groups of checks from the Calibre Interactive interface. They can also configure their own check recipes using the "Check Selection Recipe Editor" option.

Designers can also perform "Area DRC" on a select area of a large design to reduce translation time and cut verification cycle time during debugging.



Check recipes are an effective way to repetitively run selected checks.



Runsets simplify set-up and ensure consistency.

Layout vs. Schematic Checking

When invoked from supported design environments using the Calibre Interactive interface, the Calibre LVS tool automatically translates layout data to GDSII and schematics to netlist. It also enables users to isolate shorts by layer and by cell.

Parasitic Extraction

From the Calibre Interactive interface, designers can control parasitic extraction variables in the Calibre xRC or Calibre xACT tools, select the type of parasitics to extract (C, RC, and/or RCC), and specify a run on a selected net. They can also choose to output a netlist to HSPICE, DSPF or CalibreView formats, which can be used to generate an extracted schematic view inside the Cadence DFII or OpenAccess database. Designers may configure simulation testbenches to reference the CalibreView data to include the parasitic effects in their simulation output.

Results Viewing

The Calibre RVE results viewing environment offers visualization for debugging Calibre verification results. The Calibre RVE tool highlights errors found by Calibre nmDRC, nmLVS, PERC, and xRC/xACT verification, and enables designers to cross-probe nets, devices, and parasitic data between native layout and schematic windows. The Calibre RVE tool also highlights errors against both the source and extracted netlists, which provides designers with more information for debugging circuits. Complex nets can be traced using the built-in Calibre RVE schematics generated from layout and source netlists.

The Calibre nm Platform

The Calibre nm Platform, the industry's leading physical and circuit verification platform, is known for delivering best-in-class performance, accuracy, and reliability. Complete Calibre sign-off rule decks and extensive coverage of Calibre processes are available at all major semiconductor foundries. Direct support of the Calibre rule decks by the foundries and independent device manufacturers (IDMs) provides comprehensive coverage for your process nodes, and ensures you have the earliest access to the rule decks that ensure first-pass silicon success. Our strong relationship with your manufacturer ensures you can deliver tapeouts with Calibre confidence in the results.

For the latest product information, call us or visit: w w w . m e n t o r . c o m

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