Questa Verification IP

Built for Fastest Time to Verification Sign-Off

Mentor's Questa® Verification IP (QVIP) integrates seamlessly into all advanced verification environments on any simulator. With a consistent and easy-to-use UVM architecture across all protocols, QVIP ensures maximum productivity and flexibility for the verification of block level, subsytem, and SoC designs.

Today's designs rely heavily on a growing variety of complex industry standard interface protocols. QVIP enables engineers to effectively deal with this complexity, improves quality, and reduces schedule time by building Mentor's protocol and methodology expertise into a library of reusable components that support many industry standard interfaces. This frees engineers from spending time developing BFMs, verification components, or VIP, so they can focus on the unique and high-value aspects of their designs.
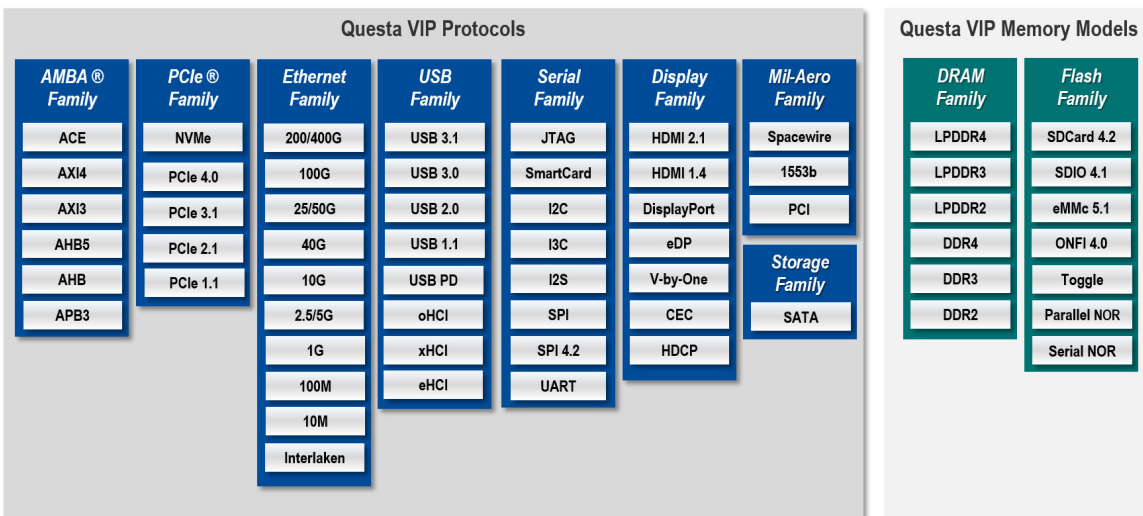
Large Library of Protocols and Memory Models

QVIP supports a large library of industry-standard protocol and memory interfaces and devices. It includes standard SystemVerilog UVM components using a consistent, common architecture that allows rapid deployment and sharing of multiple protocols and memory models within a verification team. Test plans, compliance tests, test sequences, and protocol coverage are all included as SystemVerilog and XML source code, allowing easy reuse, extension, and debug. All QVIP components include a comprehensive set of protocol checks, error injection, and debug capabilities.

FEATURES AND BENEFITS

- Consistent UVM architecture

- Easy-to-use EZ-VIP API

- Fast bring up: less than a day even for advanced serial protocols, such as PCI Express®

- Responsive, expert support 24/7

- Supported on all simulators

- Comprehensive test suite and compliance tests

- Complete verification plan, protocol coverage, and checking

- Intuitive transaction-level debug

- High-quality, mature VIP validated against commonly used design IP
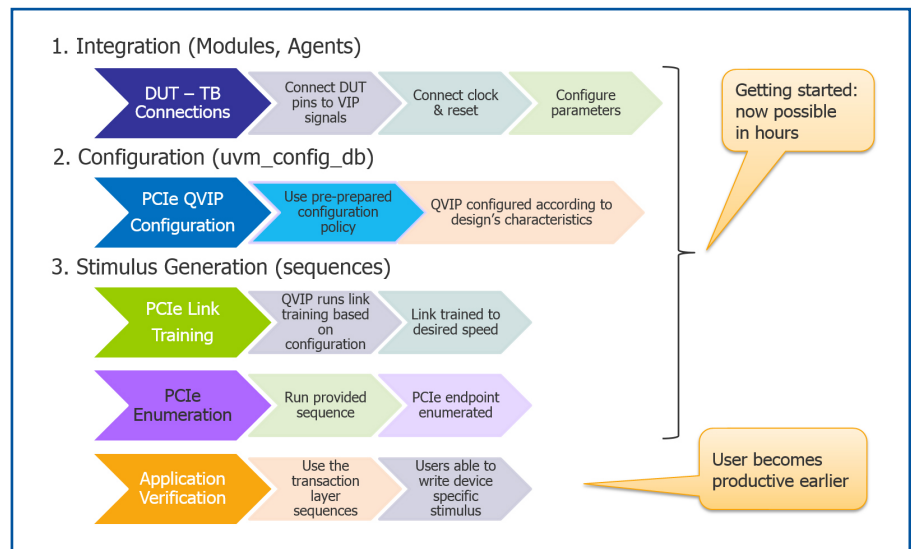
QVIP Library of Protocols and Memory Models

Questa VIP Protocols							Questa VIP Memory Models	
AMBA ® Family	**PCIe ® Family**	**Ethernet Family**	**USB Family**	**Serial Family**	**Display Family**	**Mil-Aero Family**	**DRAM Family**	**Flash Family**
ACE	NVMe	200/400G	USB 3.1	JTAG	HDMI 2.1	Spacewire	LPDDR4	SDCard 4.2
AXI4	PCIe 4.0	100G	USB 3.0	SmartCard	HDMI 1.4	1553b	LPDDR3	SDIO 4.1
AXI3	PCIe 3.1	25/50G	USB 2.0	I2C	DisplayPort	PCI	LPDDR2	eMMc 5.1
AHB5	PCIe 2.1	40G	USB 1.1	I3C	eDP		DDR4	ONFI 4.0
AHB	PCIe 1.1	10G	USB PD	I2S	V-by-One	**Storage Family**	DDR3	Toggle
APB3		2.5/5G	oHCI	SPI	CEC	SATA	DDR2	Parallel NOR
		1G	xHCI	SPI 4.2	HDCP			Serial NOR
		100M	eHCI	UART				
		10M						
		Interlaken						

Mentor®
A Siemens Business

EZ-VIP: Architected for Rapid Productivity

EZ-VIP APIs and quick starter kits take care of the tedious connection, configuration, and set up tasks, so engineers can start writing tests using QVIP within a day, even for complex serial protocols, such as PCI Express and USB.
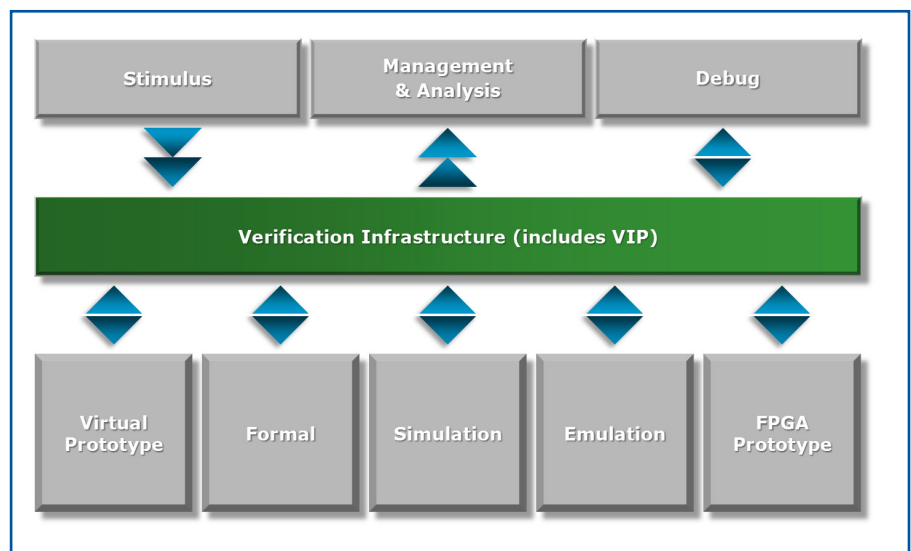
- Reusable protocol test plans linked to supplied protocol coverage
- Complete protocol checks and test suites achieve 100 percent protocol coverage to verify protocol compliance
- Comprehensive VIP built using advanced methodologies for fastest time to verification sign-off

1. Integration (Modules, Agents)

DUT – TB Connections → Connect DUT pins to VIP signals → Connect clock & reset → Configure parameters

2. Configuration (uvm_config_db)

PCIe QVIP Configuration → Use pre-prepared configuration policy → QVIP configured according to design's characteristics

3. Stimulus Generation (sequences)

PCIe Link Training → QVIP runs link training based on configuration → Link trained to desired speed

PCIe Enumeration → Run provided sequence → PCIe endpoint enumerated

Application Verification → Use the transaction layer sequences → Users able to write device specific stimulus

Getting started: now possible in hours

User becomes productive earlier

Three Steps to Productivity with VIP: Integrate > Configure > Generate Stimulus > Verify Product

An Integral Part of the Enterprise Verification Platform

Mentor Graphics Verification IP is a key component of the Enterprise Verification Platform™ (EVP). Complete VIP components reduce bring up time and enable rapid coverage closure. Common APIs and methodologies enable tests and testbenches to be moved from one verification engine to another. As an integral part of EVP, QVIP can be used with a combination of shared databases, debug applications, and analysis tools, allowing users to choose the best tool for different tasks within a single, highly productive verification flow.

Stimulus | Management & Analysis | Debug

Verification Infrastructure (includes VIP)

Virtual Prototype | Formal | Simulation | Emulation | FPGA Prototype

The Enterprise Verification Platform